REMARKS

This Response to Office Action is submitted in response to the outstanding Office Action, dated September 1, 2009. The present application was filed on February 26, 2004 with claims 1 through 20. Claims 1-3, 6-9, 12-16, 19, and 20 were cancelled in previous responses. Claims 4, 5, 10, 11, 17, and 18 are presently pending.

In the Office Action, the Examiner objected to the specification and rejected claims 4-5, 10-11 and 17-18 under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. (United States Patent No. 6,493,770) and further in view of Adams et al. (United States Patent No. 5,987,568).

Formal Objection

In the Office Action, the Examiner objected to the specification for containing embedded hyperlinks. The specification was previously amended to convert the embedded hyperlinks to *regular text*. Applicants submit that the inserted reference to the web site *where the article can be found* is a valid citation and ***not*** an embedded hyperlink, in a similar manner to a reference to a publication in an article. Applicants submit, in fact, that it is required to provided an indication of *where the article can be found.*

Applicants respectfully request withdrawal of the objection.

Independent Claims 5, 11 and 18

Independent claims 5, 11, and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sartore et al. and further in view of Adams et al. With regard to claims 5, 11, and 18, the Examiner asserts that Sartore teaches an integrated controller for use in a peripheral device for controlling high speed communications (citing element 71, FIG. 2) between a host computer (element 52, FIG. 2) and said peripheral device (element 54, FIG. 2), comprising: a processor (element 72, FIG. 2) integrated with said controller for controlling communications on a bus using one or more communication functions (col. 5, lines 18-23), wherein said processor performs at least one function for said peripheral device in addition to said one or more communication functions (col. 5, lines 25-35).

The Examiner acknowledges that Sartore does not provide details on functions of the peripheral. The Examiner alleges that it would be inherent that the CPU controls at least one

function of the peripheral device. The Examiner asserts that Adams teaches a single processor in a peripheral performing functions of the peripheral device.

As discussed hereinafter, the CPU 72 in the peripheral 54 of Sartore does not "perform at least one function for said peripheral device *in addition to* said one or more communication functions," as required by the independent claims. Rather, it is clear that the CPU 72 in Sartore is only used to *reconfigure* the peripheral over a USB interface 71. The CPU 72 is not used for the normal operation of the peripheral.

As indicated in the Abstract of Sartore (emphasis added):

> A system and method for *reconfiguring* a peripheral device connected by a computer bus and port to a host from a *first* generic configuration to a *second* manufacturer specific configuration is provided in which the configuration of a peripheral device may be electronically reset. A peripheral interface device for a standardized computer peripheral device bus and port is also provided in which a physical disconnection and reconnection of the peripheral device is *emulated to reconfigure* the bus and port for a particular peripheral device.

See, also, col. 5, lines 23-25, where it is noted that memory 74 may initially contain an identification code to indicate which *configuration information* set should be *downloaded* to the peripheral device.

Thus, among other limitations, the CPU 72 of Sartore does not disclose or suggest performing at least one function for said peripheral device *in addition to* said one or more communication functions, or *provide* ***processing capacity for use by*** *said peripheral device*, as required by each independent claim.

Adams is cited for a processor in a peripheral for performing and controlling functions of the peripheral. Adams does not disclose or suggest a processor *integrated with said controller* for performing at least one function for said peripheral device *in addition to* said one or more communication functions, or *provide* ***processing capacity for use by*** *said peripheral device*, as required by each independent claim.

Applicants respectfully request the withdrawal of the rejection of pending claims 4, 5, 10, 11, 17, and 18. Dependent Claims 4, 10, and 17, are dependent on independent claims 5, 11 and 18, and are therefore patentably distinguished over Sartore et al. and Adams et al., alone or in combination, because of their dependency from independent claims 5, 11 and 18 for

the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 4, 5, 10, 11, 17, and 18, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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